



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/885,434

06/19/2001

William J. Benett

IL-10473

4213

7590

09/07/2004

Alan H. Thompson
Assistant Laboratory Counsel
Lawrence Livermore National Laboratory
P.O. Box 808, L-703
Livermore, CA 94551

EXAMINER

MANDALA, VICTOR A

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/885,434

Applicant(s)

BENETT ET AL.

Examiner

Victor A Mandala Jr.

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4,5,8,10-18,21-23,26,29,31 and 32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15-17 is/are allowed.
- 6) ☒ Claim(s) 1,11-13,18,23 and 31 is/are rejected.
- 7) ☒ Claim(s) 4,5,8,10,14,21,22,26,29 and 32 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 11-13, 18, 23, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,441,119 Link.

5. Referring to claim 1, a connector chip for electrically connecting a conductive contact pin thereto, comprising: a non-conducting top layer, (Figure 1 #66); a non-conducting bottom layer, (Figure 1 #32); a conductive sheet, (Figure 1 #50), situated between the top layer, (Figure 1 #66), and the bottom layer, (Figure 1 #32); and a passageway, (Figure 1 #62), extending at least partially through the chip, (Figure 1 #10), the passageway including flexible cantilever means, (Figure 1 #50), for holding the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), in contact with the sheet, (Figure 1 #50), and for restraining the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), from translating with respect to the chip, (Figure 1 #10), said cantilever, (Figure 1 #50 where it is in the vertical direction), means being curvilinearly deflectable by the pin so as to produce a normal force against a lateral side of the pin and an associated frictional force which resists withdrawal of the pin from the passageway, (Figure 1 #50 where #50 will curvilinearly deflect away from its normal position to enable the pin to be inserted and have a frictional force applied to the pin so an electrical contact can be made).

Art Unit: 2826

14. Referring to claim 11, the electrical connector chip comprising means for preventing rotation of the pin with respect to the chip, (Figure 1 shows an array of slotted holes, which receive an array of pins. This array would lock the chip to the pins and not allow the any rotation to occur. The friction from #50 in Figure 1 would also not allow the pin to rotate).

15. Referring to claim 12, the electrical connector chip further comprising: a plurality of passageways, (Figure 1 #62), through the chip, (Figure 1 #10); and a harness, (Col. 5 Lines 18-20), including a plurality of pins spatially arranged so that each of the pins can be simultaneously aligned with one of the passageways, respectively, whereby all of the pins can be simultaneously inserted into passageways, (Figure 1 #62), respectively, and the harness is prevented from translating or rotating relative to the chip by holding means when the contact pins are respectively inserted into the passageways, (Figure 1 shows an array of slotted holes, which receive an array of pins. This array would lock the chip to the pins and not allow the any rotation to occur. The friction from #50 in Figure 1 would also not allow the pin to rotate).

16. Referring to claim 13, the electrical connector chip wherein: each cantilever, (Figure 1 #50), means is electrically isolated from the other cantilever, (Figure 1 #50), means and is electrically connected to a respective chip element, (Figure 1 #52 to #26), whereby each chip element, (Figure 1 #26), is connected to a respective contact pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), when the contact pins, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), are respectively inserted into the passageways, (Figure 1 #62).

19. Referring to claim 18, the method for electrically connecting a chip and a conductive contact pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), comprising mechanically holding, (Figure 1 #50), the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), in a

Art Unit: 2826

passageway, (Figure 1 #62), in the chip, (Figure 1 #10), by the curvilinear deflection of a flexible cantilever means, (Figure 1 #50), when the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), is inserted into the passageway, (Figure 1 #62), wherein the curvilinear deflection of the flexible cantilever means, (Figure 1 #50), produces a normal force against the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), and an associated frictional force to resist withdrawal of the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), and wherein the mechanical hold, (Figure 1 #50), establishes and maintains an electrical connection between the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), and an electrical element, (Figure 1 #26), embedded in the chip, (Figure 1 #10) and (Figure 1 #50 where #50 will curvilinearly deflect away from its normal position to enable the pin to be inserted and have a frictional force applied to the pin so an electrical contact can be made).

24. Referring to claim 23, a connector of a chip of a type having passageway, (Figure 1 #62), extending at least partially there through, for electrically connecting a conductive contact pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), to the chip, (Figure 1 #10), the connector comprising: a conductive sheet, (Figure 1 #50), having a peripheral portion connected to the chip, (Figure 1 #10), adjacent the passageway, (Figure 1 #62), and flexible cantilever means, (Figure 1 #50), extending from the peripheral portion into the passageway, (Figure 1 #62), to at least one unsupported end, said flexible cantilever means, (Figure 1 #50), being curvilinearly deflectable by the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), so as to produce a normal force against the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), and an associated frictional force which resists withdrawal of the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), from the passageway, (Figure 1 #62), for holding a pin,

Art Unit: 2826

(Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), in contact with the sheet, (Figure 1 #50), and for restraining the pin, (Figure 1 area to receive pin #62 & Col. 5 Lines 18-20), from translating with respect to the chip, (Figure 1 #10) and (Figure 1 #50 where #50 will curvilinearly deflect away from its normal position to enable the pin to be inserted and have a frictional force applied to the pin so an electrical contact can be made).

32. Referring to claim 31, the electrical connector of the chip comprising means for preventing rotation of the pin with respect to the chip, (Figure 1 shows an array of slotted holes, which receive an array of pins. This array would lock the chip to the pins and not allow the any rotation to occur. The friction from #50 in Figure 1 would also not allow the pin to rotate).

Allowable Subject Matter

Claims 4, 5, 8, 10, 14, 21, 22, 26, 29, and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15-17 are allowed.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent Nos. 4,953,060 Lauffer et al. & 4,342,069 Link.

Art Unit: 2826

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9330.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

VAMJ
8/27/04